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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/591,225
Filing Date: June 09, 2000
Appellant(s): BALDWIN, DAVID ROBERT

Patrick C.R. Holmes

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 19, 2007 appealing from the Office action mailed September 19, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

EP 0766177 Kaiser 4-1997

Jim Blinn's Corner, "The Truth About Texture Mapping" by James Blinn, IEEE Computer Graphics & Application, 3/1990, Pages 78-83.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-5, 7-10, and 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaiser (European Patent Publication 0 766 177) in view of Blinn (Jim Blinn's Corner "The Truth About Texture Mapping").

(10) Response to Argument

A1. With respect to claims 1, 2, 4, 5, 7-10, 12, 13, and 16-22, appellant argues that virtual address translation is not the same as a page fault and that Kaiser requires the host processor to handle a page fault.

Appellant argues that Kaiser handles virtual address translation without host processor involvement, which examiner agrees with. Though appellant never explicitly defines the term "page fault" in the specification, appellant further argues that virtual address translation and page faults have different definitions in both appellant's application and the Kaiser reference. This ignores the broadest reasonable definition of the term "page fault", which as pointed out in the Advisory Action, can read on a "miss" of the TLB:

Applicant argues that the TLB miss described by Kaiser does not read on a "page fault", and that when an actual page fault occurs in Kaiser, it is not handled invisibly to the host processor. However, after further researching the broadest reasonable definition of a "page fault", examiner has concluded that a TLB miss does meet such a definition. Nothing in the claims or specification of the instant application specifically excludes such a miss from being considered a "page fault", and examiner has found evidence that such a TLB miss is sometimes referred to as a "page fault" by one skilled in the art. For instance, a reference from the computer science department of USC, available at http://www-scf.usc.edu/~csci402/assignment3/project3_doc.html, states that a TLB miss in NACHOS generates a "PageFaultException" and that handling this "page fault" includes putting a particular virtual address-physical address translation into the TLB. See in particular paragraphs 2-5 of the reference, under the heading "The TLB". Another reference, available on the University of Waterloo's website (http://bcr2.uwaterloo.ca/~brecht/courses/4321/handouts/vm.ps) confirms this, stating in paragraph 4 that a TLB exception in NACHOS generates a "PageFaultException". Note that these references are only being used to show known definitions of a "page fault" and therefore are not being applied as prior art references. MPEP 2163 states that "Each claim must be separately analyzed and given its broadest reasonable interpretation in light of and consistent with the written description." Since it is known in the art that a TLB miss can be considered a page fault,

and the application does not limit the definition of "page fault" to exclude a TLB miss, examiner has concluded that the TLB miss of Kaiser does anticipate a broadly claimed "page fault".

Even comparing a "TLB miss", which occurs if virtual address translation cannot be performed with the TLB, to the definition of a "page fault" that appellant would like examiner to use, there are many similarities. The Kaiser invention attempts to perform virtual address translation by comparing an effective address to the addresses in the TLB (col. 5, lines 45-58). If no address matches, the memory controller fetches lines from the system page table. Since this process is handled by the controller with no interaction between the controller and the host processor, this process is performed invisibly to the host processor. The host processor is only involved if no entry is found in the system page table.

Compare this to appellant's "page fault" process, which is described on page 8 of applicant's specification: Appellant's invention attempts to find a texture page in a first level of memory, analogous to Kaiser's TLB. When a page of texture is not found in the first level of memory, the graphics memory manager, analogous to Kaiser's memory controller, updates page tables by replacing the least-recently used page with the fetched page, invisibly to the host processor. Here, the fetched page is analagous to the lines fetched from the system page table in Kaiser. If the page does not exist in second level memory, appellant's invention involves the host processor and fetches the page, analogous to how the Kaiser reference involves the host processor if no entry is found in a system page table. Thus, even if the examiner used the definition of "page fault" that appellant would like to be used, which would be too narrow, as shown above,

one skilled in the art would still recognize Kaiser's "TLB miss" to be very similar to appellant's "page fault", necessitating a 35 USC 103 rejection of appellant's claims.

A2. With respect to claims 1, 2, 4, 5, 7-10, 12, 13, and 16-22, appellant further argues that Nachos eliminates the page table and replaces it with a TLB, and is thus not analogous to Kaiser.

Appellant uses "Nachos" to refer to the reference used to support examiner's definition of the term "page fault", available at http://www-scf.usc.edu/~csci402/assignment3/project3_doc.html. Appellant argues that the page table does not exist in Nachos and because Nachos is a host, the TLB miss in Nachos is equivalent to a "page fault", but also argues that the Kaiser TLB miss is not similar because is merely an address translation miss. However, examiner notes that there is indeed a page table discussed on page 2 of this reference under the heading "The IPT", which discloses an inverted page table. This appears analogous to the Kaiser reference as a TLB exists in that reference also, and a page table is used only when there is a TLB miss.

Also, note the other Nachos reference that was cited: http://bcr2.uwaterloo.ca/~brecht/courses/4321/handouts/vm.ps. This reference notes on page 1, paragraph 2, that "if the mapping is not in the TLB (a TLB "miss"), page tables and/or segment tables are used to determine the correct translation". This reference further states, on page 1, paragraph 4, "When a program references a page that is not in the TLB, the hardware generates a TLB exception (in Nachos a PageFaultException), trapping to the kernel. The operating system then checks its own page table." This

reference more clearly shows that a TLB miss is considered a "page fault" even when the operating system then checks its page table.

A3. With respect to claims 1, 2, 4, 5, 7-10, 12, 13, and 16-22, appellant further argues that the Nachos reference was not cited until the Advisory Action, and thus reliance on the reference is improper.

Examiner notes that the reference was not relied upon to reject claims 1, 2, 4, 5, 7-10, 12, 13, and 16-22, and thus this is a moot point. Instead, the Nachos reference was cited only for evidentiary support of the examiner's previous statement that a TLB miss could be equivalent to a page fault. The applicant challenged examiner's interpretation of the term "page fault" on pages 1-3 of the Remarks filed December 19, 2006 in response to the Final Office Action mailed out on September 19, 2006. The examiner noted these arguments in the Advisory Action filed January 23, 2007, as required. Responding to this challenge, it was absolutely necessary for the examiner to cite extrinsic evidentiary support for examiner's assertions.

See MPEP 2111.01, which explains that the words of a claim are given their plain meaning unless such meaning is inconsistent with the specification. MPEP 2111.01 goes on to state that "It is the use of the words in the context of the written description and customarily by those skilled in the relevant art that accurately reflects both the "ordinary" and the "customary" meaning of the terms in the claims." This section of MPEP further states that "The ordinary and customary meaning of a term may be evidenced by a variety of sources including 'the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence

concerning relevant scientific principles, the meaning of technical terms, and the state of the art.'" The examiner is therefore correct in gleaning the definition of the term "page fault" from external sources such as the Nachos references. These references simply show a broad definition of a "page fault" and are not used to actually teach the limitations of the claims.

B1. With respect to claims 3, 14, and 15, appellant argues that Kaiser does not show a dedicated graphics memory.

Examiner had previously cited the page buffer found in figure 2 of Kaiser as a dedicated graphics memory. Appellant argues that this buffer is part of the memory controller where address translations are stored. Appellant further argues that a "dedicated graphics memory" is used primarily or only by a graphics processor. In this instance, examiner notes that appellant has attempted to give the term "dedicated graphics memory" a definition that is narrower than the broadest reasonable interpretation of the term. There is nothing about a "dedicated graphics memory" that necessarily implies use by a graphics processor. A "dedicated graphics memory", given its plain meaning, is simply a memory that is dedicated to graphics. Nevertheless, the Kaiser reference does specifically reference an "auxiliary function processor" in col. 1, lines 5-9, and further states that this may be a "graphics processor" in col. 5, lines 13-25 and element 206 in figure 2. Looking again to figure 2, it is clear that the page table buffer 226 is read by the graphics processor 206, and *not* other processors, using the table walk logic 224. Thus, it is proper to assume that the page buffer will contain only entries dedicated to graphics rather than other data.

B2. With respect to claims 3, 14, and 15, appellant further argues that Kaiser does not teach or suggest a second memory management unit.

Appellant argues that this limitation is not addressed in the rejection to claims 1 and 2 and also that the page buffer of figure 2 cannot be a second memory management unit. However, taking another look at claim 3, examiner notes that appellant does not actually claim two different memory management *units*. Appellant instead claims a first memory *logic*, as in line 4 of claim 3, line 3 of claim 14, and line 3 of claim 15, and a second memory management *unit*, as in line 7 of claim 3, line 8 of claim 14, and line 7 of claim 15. Logic is a broad term, and could encompass anything from a program to a logic circuit. Col. 1, lines 13-45 of Kaiser explain that virtualization of a main memory is done, and since the Kaiser reference deals with a computer, it must be done with some sort of logic, that being a program or circuit. Thus, a first logic executing this task is inherent to the Kaiser reference. The second memory management unit corresponds to the memory controller in figure 2, which is also discussed in claims 1 and 2. Note that none of these claims contain a first memory management unit separate from the second memory management unit.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Aaron M. Richer

Conferees:

Aaron M. Richer

Kee Tung

Ulka Chauhan

KEE M. TUNG
SUPERVISORY PATENT EXAMINER